Do NOT ENTER A1 (KEEP ORIGINAL ABSTRACT)

ABSTRACT

Apparatus and methods for controlling the sensing of bit lines which facilitates the distribution of bit line charging current to be distributed any time, and facilitates the fast raising of the sense modes to full logic levels. An embodiment is comprised of a plurality of bit storage capacitors, a folded bit line for receiving charge stored on one of the capacitors, having bit line capacitance, a sense amplifier having a pair of sense nodes for sensing a voltage differential across the sense nodes, apparatus connected to the bit line and the sense nodes for imperfectly isolating the sense nodes from the bit line whereby current can leak therethrough, apparatus for enabling the sense amplifier and for disabling the isolating apparatus and thereby removing the isolation between the sense amplifier and the bit line, whereby current passing through the sense amplifier to the sense nodes is enabled to charge the bit line capacitance through the isolating apparatus to predetermined logic voltage level.

In the Claims

Please amend Claim 25.

A2

25. (Amended) A method is claimed in claim 24 wherein the active high logic level and active low logic level are applied to inputs of the bit line sense amplifier through local transistors connected to voltage source power tracks and gated by logic signals.

REMARKS

Claims 18-25 are pending in the Application, which is a Continuation of reissued U.S. Patent No. RE37641. Claims 1-17 are canceled. All pending claims have been rejected, as discussed below.

1. Although the Examiner states that this Application is a reissue of U.S. 5,414,662, Applicants note that this Application is a Continuation of U.S. RE37641, which is a reissue of U.S. 5,414,662.